HP 3000 SERIES II
COMPUTER SYSTEM
MANUAL OF STAND-ALONE DIAGNOSTICS

STAND-ALONE
HP 30008A/30009A ERROR CORRECTION
MEMORY DIAGNOSTIC

Diagnostic D430A

30008-90001
Printed in U.S.A.

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I. INTRODUCTION

The Stand-Alone Series II Memory Subsystem with Fault Correction Diagnostic (D430A) performs the following:

- Verifies 'FLI' array, reads the previous history of both 'MCL' arrays (lower 128K and upper 128K) and lists all errors.
- Clears and verifies both 'MCL' arrays.
- Verifies all available 'SMA' arrays and lists any detected error.
- Checks the capability to detect and correct single errors in both data and check bits as well as to detect most 'multi-errors' and the I/O failures in 'PCA' array.
- Executes the main diagnostic program for all 'SMA' arrays.
- Reads and lists the error history of both 'MCL' logging arrays

The diagnostic is used by field service, system test, and manufacturing personnel to detect and isolate chip error on any 4K RAM memory array (SMA).

NOTE: MCL = Memory Control Logging
FLI = Fault Logging Interface
SMA = Semiconductor Memory Array
FCA = Fault Correction Array

II. MINI-OPERATING INSTRUCTIONS

1. COLD LOAD DIAG FILE # FROM NON-CPU COLD LOAD TAPE
   # AFTER HALT SET SWITCH OPTIONS FOLLOWED BY 'CR' TO CONTINUE
2. HP 3000 SERIES II ERROR CORRECTING MEMORY TEST D430A.XX.Y
3. SØ INDICATES NO ERROR IN LLA.
4. SØ INDICATES NO ERROR IN ULA.
5. LOWER BANK?
6. LOWER ADDRESS? (SHOULD NOT BE 0)
7. UPPER BANK?
8. UPPER ADDRESS?
   # AFTER ALL ENTRIES HAVE BEEN MADE, PRESS 'CR' TO START DIAGNOSTIC.

BIT	SWITCH REGISTER OPTIONS:
0	SELECT EXTERNAL REGISTER
1	CALL SERVICE TO RESTART
2	LOOP ON CURRENT STEP
3	EXECUTE SHORTER PART IN SECTION 5
4	EXECUTE "MARCHING" IN SECTION 5
5	EXECUTE "READ/WRITE HAMMER" IN SECTION 5
6	EXECUTE "DIAGONAL" IN SECTION 5
7	EXECUTE "PING-PONG" IN SECTION 5
8	SKIP CURRENT SECTION OR STEP
9	SUPPRESS E-CLASS MESSAGES (ERRORS)
10	SUPPRESS D-CLASS MESSAGES (NON-ERRORS)
11	LOOP ON CURRENT SECTION
12	HALT ON ERROR
13	HALT AT THE END OF CURRENT STEP
14	HALT AT THE END OF CURRENT SECTION
15	HALT AFTER DIAGNOSTIC PASS

BITS:12,13,14,15	HALT CODE
HALT CODE 00	MEANS: MEANING OR ACTION REQUIRED
HALT CODE 01	ILLEGAL INTERRUPT TO STT
HALT CODE 05	PARITY ERROR IN PROGRAM AREA
HALT CODE 10	TRAPPED IN SEGMENT 2 OR SEGMENT 4
HALT CODE 12	TRANSFER ERROR DURING RELOCATION'1
HALT CODE 13	TRANSFER ERROR DURING RELOCATION'2
HALT CODE 14	ERROR HALT
HALT CODE 15	END OF STEP
HALT CODE 16	END OF SECTION
HALT CODE 17	END OF TEST

III. REQUIREMENTS

A. Hardware

1. Minimum System HP 3000 Series II CPU
2. HP 30008A/30009A Error Correction Memory Diagnostic

B. Software

1. Non CPU Cold Load Tape #30000-10017/11017

IV. DETAILED OPERATING INSTRUCTIONS

A. Operating Instructions

1. Loading

To load the diagnostic refer to loading procedure in the SDUPII Mod 03000-90125.

2. Running

A. Upon completion of a successful load, the following messages are printed at the control terminal:

```
HP 3000 SERIES II ERROR CORRECTING MEMORY TEST D430A
EØ.Ø2 UPPER MCL, NOT RESPONDING  (*)
LOWER BANK?
```

B. Input the lowest bank to be tested followed by 'CR' to continue. The next message printed is:

```
LOWER ADDRESS?
```

C. Input the lowest address of a lower bank to be tested followed by 'CR' to continue. If the lower bank = Ø the input has to be any number higher than zero. The following message is then printed:

```
UPPER BANK?
```

D. Input the number of the highest bank to be tested followed by a 'CR' to continue. The next message printed is:

```
UPPER ADDRESS?
```

(*) Indicates upper banks (2 and 3)

A. Operating Instructions (continued)

E. Input the number of the highest address of the higher bank to be tested followed by 'CR' to execute the diagnostic. The execution of the program takes approximately 180 minutes for each fully tested bank. If no serious error problems arise, the following messages are printed:

D6.65 NO ERROR IN LOWER MCL
D6.65 NO ERROR IN UPPER MCL
D6.65 XX PASS

F. It means that the execution of diagnostic was finished in all sections and if no halt at pass is requested (switch 15 set), the next run starts.

3. Control Change to Restart

A. Set switch 0 and 1. The follwoing message is printed:

RESTART? (YES/NO)

4. Skipping Sections and Looping Current Section

A. Halt execution, set switches 0, 8 (skip current step or section) and 14 (halt at end of current section). Then start 'RUN'. The following messages are printed by each pressing of 'RUN':

DX.YY HALT AT END OF SECTION X.

B. X is the number of skipped section and the test operator steps sections up to the required number by pressing 'RUN' until desired section is reached.

A. Operating Instructions (continued)

C. Reset switch 8 (skipping) and optionally reset switch 14 (halt at end of current section) and set switch 11 (loop on current section).

5. Skipping Steps

A. Halt execution, set switches 0, 8 (skip current step or section) and 13 (halt at end of current step). Then press 'RUN'. The following messages are printed each time 'RUN' is pressed:

DX.YY HALT AT END OF STEP YY.

B. X is the number of the current section and YY is the number of steps to be skipped. The test operator advances the required number of steps by pressing 'RUN' until the desired step is reached.

C. Reset switch 8 (skipping) and optionally set/reset others to continue.

B. Options

The internal switch register is used to specify program options during execution of the test. The internal switch register is loaded from the external switch register whenever switch zero of the external switch register is set. This means that the external register is free for other uses during the test, e.g., breakpoint halts.

Another switch setting that requires explanation is switch 1. If this switch is set, the program initiates a dialogue with the

B. Options (continued)

operator MESSAGE 'RESTART? (YES/NO)' . The object of this dialogue is to ask the operator to restart the program (if he wishes it for any reason).

Each section is divided into steps and the step numbers are displayed as the fraction of the section number. For example:

D4.03 HALT ON ERROR

Means halt on error at step 3 in section 4.

Table 2 SWITCH REGISTER SETTING

BIT	FUNCTION IF SET
0	SELECT EXTERNAL REGISTER
1	CALL SERVICE TO RESTART
2	LOOP ON CURRENT STEP
3	EXECUTE SHORTER PART IN SECTION 5
4	EXECUTE "MARCHING" IN SECTION 5
5	EXECUTE "READ/WRITE HAMMER" IN SECTION 5
6	EXECUTE "DIAGNOAL" IN SECTION 5
7	EXECUTE "PING-PONG" IN SECTION 5
8	SKIP CURRENT SECTION OR STEP
9	SUPPRESS E-CLASS MESSAGES (ERRORS)
10	SUPPRESS D-CLASS MESSAGES (NON-ERRORS)
11	LOOP ON CURRENT SECTION
12	HALT ON ERROR
13	HALT AT END OF CURRENT STEP
14	HALT AT END OF CURRENT SECTION
15	HALT AFTER DIAGNOSTIC PASS

C. Halt and Message Tables

Table 3 HALT CODE IN SEGMENT 3

BITS:12, 13, 14, 15	HALT CODE
HALT CODE 00	MEANS: MEANING OR ACTION REQUIRED
HALT CODE 01	ILLEGAL INTERRUPT TO STT
HALT CODE 05	PARITY ERROR IN PROGRAM AREA
HALT CODE 10	TRAPPED IN SEGMENT 2 OR SEGMENT 4
HALT CODE 12	TRANSFER ERROR DURING RELOCATION'1
HALT CODE 13	TRANSFER ERROR DURING RELOCATION'2
HALT CODE 14	ERROR HALT
HALT CODE 15	END OF STEP
HALT CODE 16	END OF SECTION
HALT CODE 17	END OF TEST

The general format of a diagnostic message to the operator is the following: A letter prefix; decimal section number (fraction means step number if any) and text. Table 4 lists messages.

The letter prefix identifies the class of the message. There are four message classes:

MESSAGE CLASS	CONTENT
D	Data information which requires no operator response.
E	Error message which indicate that disc file failed some portion of the diagnostic test.
P	Diagnostic program has paused. Waiting for operator action is performed. Enter carriage return at terminal to continue test. If messages have been supressed, press run on system control panel to continue.
Q	Input from operator at control terminal is required. Carriage return following input continues test.

C. Halt and Message Tables (continued)

EXAMPLE:

Example of printout from section 6 with listing of lower and upper logging arrays:

```
D6.46  NO ERROR IN LOWER MCL
E6.46  ERROR IN UPPER MCL
D6.46   BANK:  32K:  ROW:  BIT:
E6.46     2     U     5     12  DATA BIT
E6.46     2     U     6     A   CHECK BIT
E6.46     2     U     6   10101 MULTI ERRS
D6.46  HALT AT END OF SECTION 6
```

Table 4 MESSAGES

CLASS	MESSAGE	COMMENTS
D	HP 3000 SERIES II ERROR CORRECTING MEMORY TEST D430A.XX.Y	TITLE OF DIAGNOSTIC PROGRAM
Q	LOW BANK?	LOWEST AVAILABLE BANK FOR THE EXECUTION.
Q	LOW ADDRESS?	LOWEST ADDRESS IN THE LOW BANK FOR EXECUTION OF DIAGNOSTIC. THE NUMBER MUST BE 0.
Q	HIGH BANK?	HIGHEST AVAILABLE BANK FOR EXECUTION OF DIAGNOSTIC
Q	HIGH ADDRESS?	HIGHEST ADDRESS IN HIGH BANK.
E	NO RESPONSE TO CIO	DEVICE NUMBER SHOULD BE 2.
E	NO RESPONSE TO RIO	DEVICE NUMBER SHOULD BE 2.
E	NO RESPONSE TO TIO	DEVICE NUMBER SHOULD BE 2.
E	NO RESPONSE TO WIO	DEVICE NUMBER SHOULD BE 2.

Table 4 MESSAGES (continued)

CLASS	MESSAGE	COMMENTS
D	NO ERROR IN LOWER MCL	NO ERROR LISTED IN THE LOWER LOGGING ARRAY (BANK 0,1).
D	NO ERROR IN UPPER MCL	NO ERROR LISTED IN THE UPPER LOGGING ARRAY (BANK 2,3).
E	ERROR IN LOWER MCL	ERROR LISTING IN LOWER LOGGING ARRAY (BANK 0,1).
E	ERROR IN UPPER MCL	ERROR LISTING IN UPPER LOGGING
E	LOWER MCL, NOT RESPONDING #";	NO LOWER BANKS (0,1) OR DISCONNECTED
E	UPPER MCL, NOT RESPONDING #";	NO UPPER BANKS (2,3) OR DISCONNECTED
D	BANK: 32K: ROW: BIT:	TABLE HEAD FOR ERROR LISTING.
E	0 L 7 10 DATA BIT	SINGLE DATA ERROR
E	0 U 3 B CHECK BIT	SINGLE CHECK BIT PARITY ERROR
D	BANK: 32K: ROW: BIT:	TABLE HEAD FOR ERROR LISTING.
E	1 U 2 01010 MULTI ERRS	READ CLOCK FAILURE
E	2 L 4 01111 CHECK BIT DR.	CHECK BIT I/O DRIVE FAULT
E	1 U 2 01010 READ CLOCK	READ CLOCK FAILURE
E	LOWER MCL - VERIFY 'ZERO'	TITLE TO ERROR TABLE (SECTION 2)
E	UPPER MCL - VERIFY 'ZERO'	TITLE TO ERROR TABLE (SECTION 2)
E	FLI - VERIFY 'ZERO'	TITLE TO ERROR TABLE (SECTION Ø)
E	FLI - VERIFY 'ONE'	TITLE TO ERROR TABLE (SECTION Ø)
E	FLI - VERIFY LOAD SINGLE	TITLE TO ERROR TABLE (SECTION Ø)
	TIO WORD XXXXXX SHOULD BE YYYYYY	ERROR TABLE READ FROM MCL OR FLI ARRAY: XXXXXX IS WORD READ BY RIO AFTER READ SCAN (CIO-%10000) YYYYYY IS EXPECTED VALUE

Table 4 MESSAGES (continued)

CLASS	MESSAGE	COMMENTS
Q	RESTART? (YES/NO)	OPERATOR TYPES 'YES' TO RESTART AND 'NO' TO CONTINUE. BEFORE 'CR' SWITCH 1 SHOULD BE RESET
P	HALT AT PASS XX	XX IS OCTAL NUMBER OF PASS. PRESS 'RUN' FOR TO CONTINUE
D	XX PASS	XX IS OCTAL NUMBER
P	RESET SWITCH 1 (RESTART REQUEST)	RESET SWITCH 1 AND PUSH 'CR' FOR TO GET OUT AND CONTINUE .
E	DATA XXXXXX AT B/A Y ZZZZZZ SHOULD BE MMMMMM	XXXXXX - READDATA, Y- BANK ZZZZZZ - ADDRESS MMMMMM - EXPECTED DATA
E	FCA - CHECKING ABCDE IN SECTION 3 OBTAINED CHECK: 11111 DATA: 0 000 000 000 000 000 EXPECTED CHECK: 01111 DATA: 1 000 000 000 000 000 BANK 0 U128K ROW 8	TITLE OF ERROR CORRECTING LOGIC TEST WITH OBTAINED AND EXPECTED CHECK AND DATAS. THE LAST LINE LISTS LOCATION
P	HALT AT END OF SECTION	PRESS 'CR' TO CONTINUE
P	HALT AT END OF STEP	PRESS 'CR' TO CONTINUE
E	2 L 4 14 No LLA RST	NO CAPABILITY TO RESET ERROR BIT IN LOWER MCL ARRAY CORRESPONDING TO BIT 14 IN SMA.
E	2 L 4 14 NO ULA RST	NO CAPABILITY TO RESET ERROR BIT IN UPPER MCL ARRAY CORRESPONDING TO BIT 14 IN SMA.

D. Pre-Configuration Options

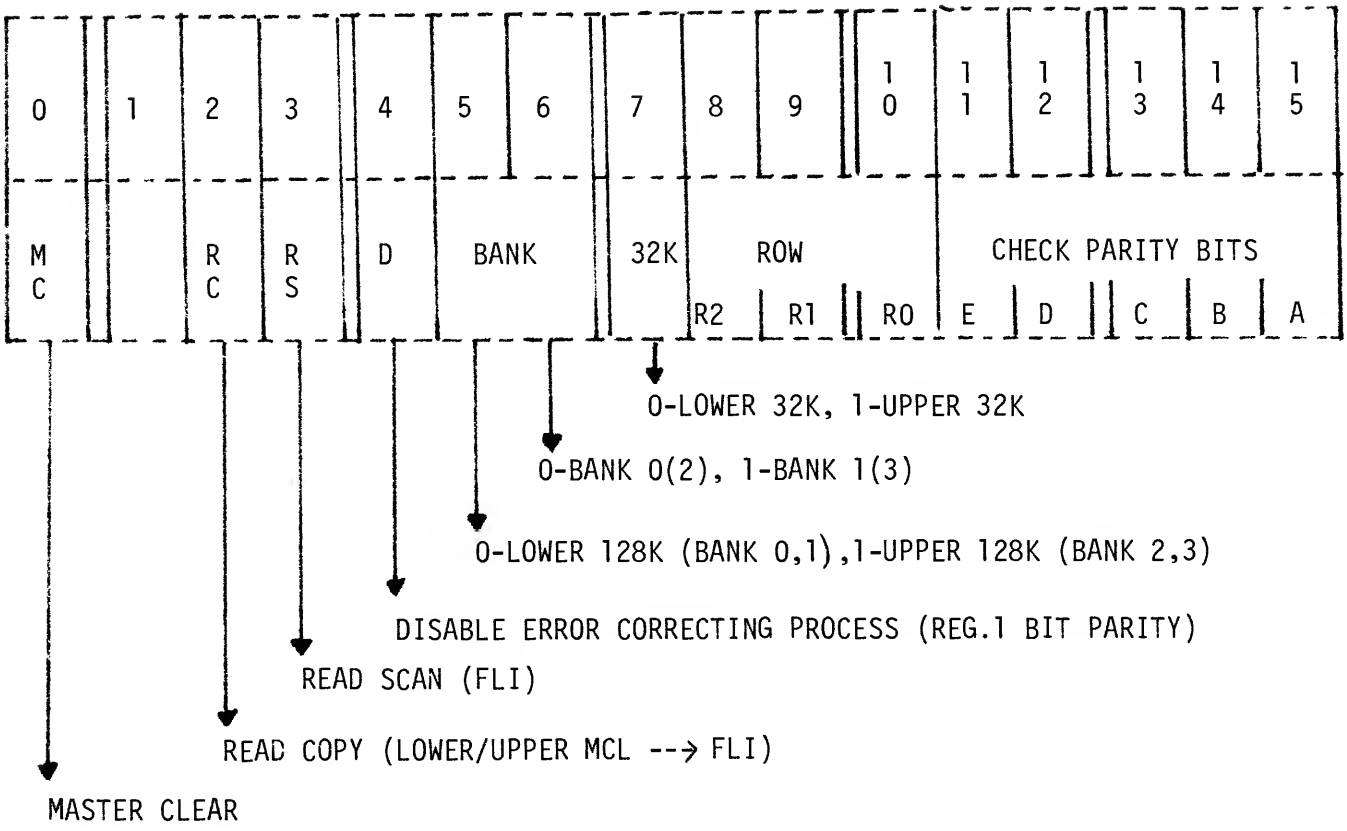
The diagnostic program has been preconfigured in the best load and go configuration using the options available from the switch register (Chapter III B). The switch register=%107400 means the run of the long cycle with all sections. The execution of one cycle with four full banks takes approximately 180 minutes.

The programmed pre-configuration (DRT of console and logging I/O board) can be altered when the diagnostic cold load tape is being created under SDUP (System Diagnostic Utility Program for HP 3000 System II).

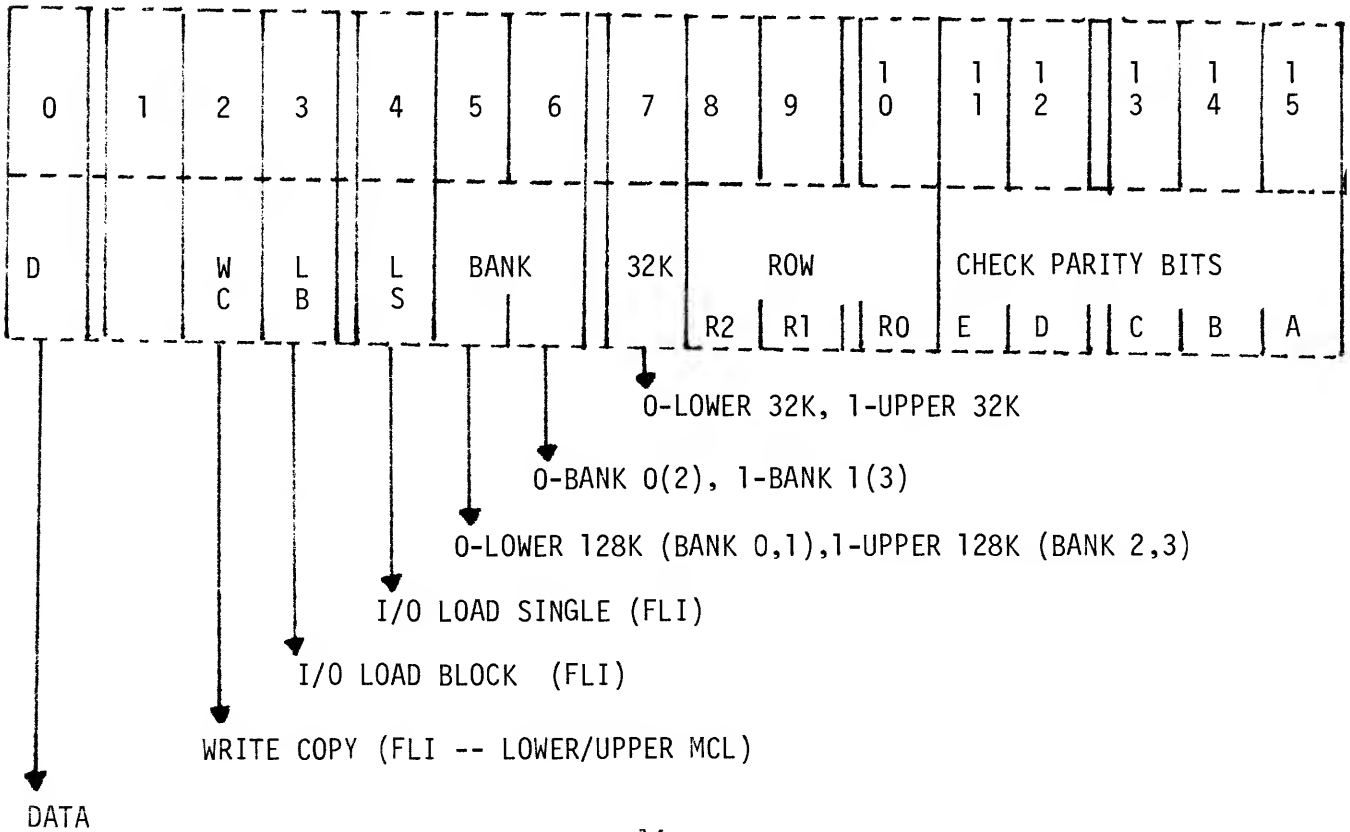
DB		PRESENT:	NOTE
DB+0	INTERNAL SWITCH REGISTER	%107400	HALT ON ERROR
DB+1	VERSION	0	A.00.0
DB+2	DEVICE NUMBER (DRT)	2	
DB+3	NUMBER OF MAX. LIST ERRORS	99	
DB+4	SECTION NUMBER	0	
DB+5	STEP NUMBER	0	

E. Direct I/O and Status Words

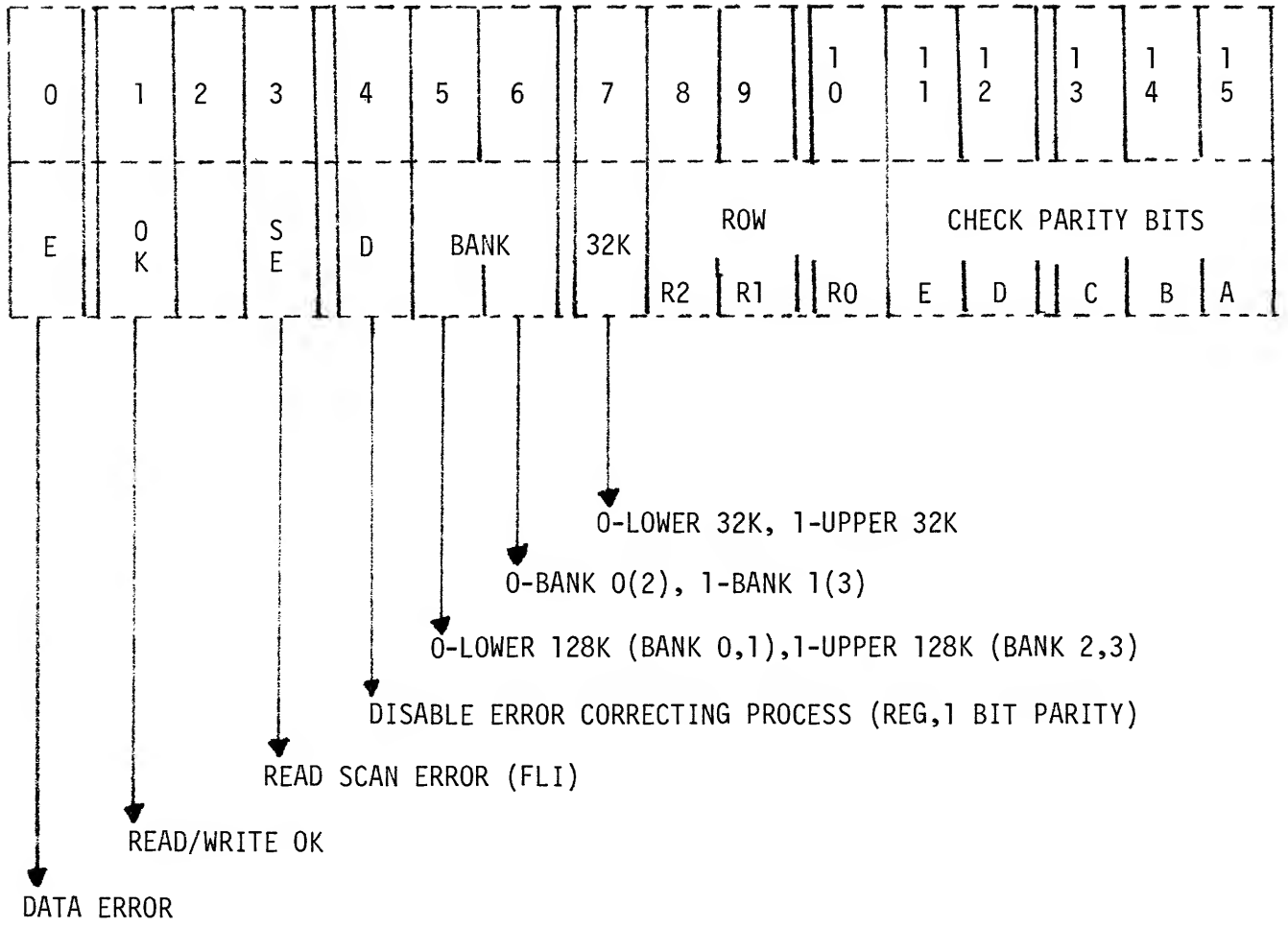
1. CIO - Format



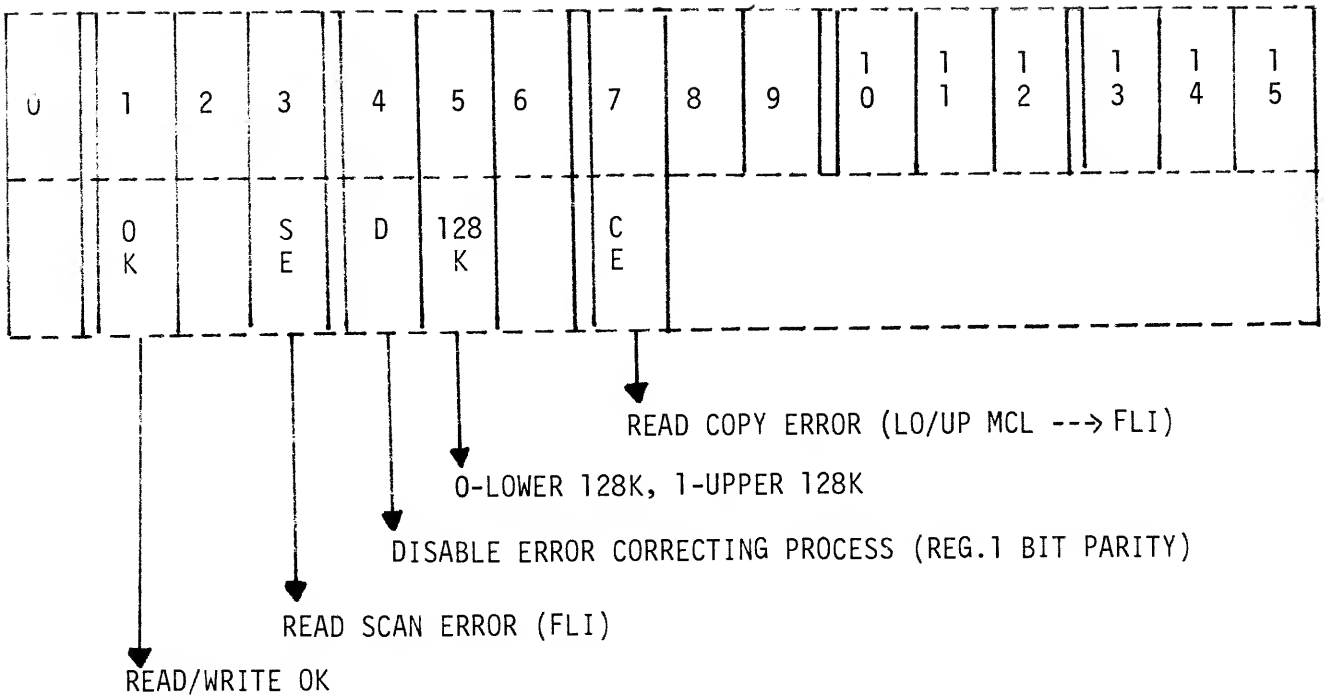
2. WIO - Format



3. RIO - Format


0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15
E
OK
SE
D
BANK
32K
ROW
R2 R1 R0
CHECK PARITY BITS
E D C B A
0-LOWER 32K, 1-UPPER 32K
0-BANK 0(2), 1-BANK 1(3)
0-LOWER 128K (BANK 0,1),1-UPPER 128K (BANK 2,3)
DISABLE ERROR CORRECTING PROCESS (REG,1 BIT PARITY)
READ SCAN ERROR (FLI)
READ/WRITE OK
DATA ERROR

4. TIO - Format


0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
OK
SE
D
128K
CE
READ COPY ERROR (LO/UP MCL --> FLI)
0-LOWER 128K, 1-UPPER 128K
DISABLE ERROR CORRECTING PROCESS (REG.1 BIT PARITY)
READ SCAN ERROR (FLI)
READ/WRITE OK

V. DETAILED DESCRIPTION OF TESTS

SECTION NAME	STEP NUMBER	FUNCTION
S0	1	VERIFIES CAPABILITY OF THE INPUT/OUTPUT LOGGING ARRAY (FLI) FOR TO WRITE/READ '0' AND '1'.
	2	READS CONTENTS OF BOTH ERROR LOGGING ARRAYS: LOWER 128K (MCL) AND UPPER 128K (MCL) AND REPORTS THE HISTORY OF THEM.
S1	3	CLEARS ALL BITS OF BOTH ERROR LOGGING ARRAYS: LOWER 128K (MCL) AND UPPER 128K (MCL).
	4	VERIFIES ALL BITS OF BOTH ERROR LOGGING ARRAYS: LOWER 128K (MCL) AND UPPER 128K (MCL).
S2	5	CLEARS BOTH ERROR LOGGING ARRAYS: LOWER 128K (MCL) AND UPPER 128K (MCL).
	6	CHECKS BOTH ERROR LOGGING ARRAYS: LOWER 128K (MCL) AND UPPER 128K (MCL) TO VERIFY THE CAPABILITY TO WRITE/READ '0' AND '1'.
	7	CLEARS BOTH ERROR LOGGING ARRAYS: LOWER 128K (MCL) AND UPPER 128K (MCL).
	10	VERIFIES ALL BITS OF BOTH ERROR LOGGING ARRAYS: LOWER 128K (MCL) AND UPPER 128K (MCL).
S3	11	WRITES 'ZEROS' INTO ALL AVAILABLE ADDRESSES IN MEMORY AND READS THEM BACK TO VERIFY THE STORE CAPABILITY.
	12	WRITES 'ONES' INTO ALL AVAILABLE ADDRESSES IN MEMORY AND READS THEM BACK TO VERIFY THE STORE CAPABILITY.
	13	RELOCATES THE PROGRAM FROM %10000 INTO %110000 IN MEMORY TO TEST THE REST OF MEMORY IN BANK 0.
	14	EXECUTES THE SAME AS STEP 11 FOR THE REST OF BANK 0.
	15	EXECUTES THE SAME AS STEP 12 FOR THE REST OF BANK 0.

SECTION NAME	STEP NUMBER	FUNCTION
S3 (cont)	16	RELOCATES THE PROGRAM FROM %110000 BACK TO %10000 IN MEMORY FOR TO CONTINUE THE DIAGNOSTIC PROGRAM.
	17	READS BOTH MCL AND LISTS ANY DETECTED ERROR.
	20	NOT USED.
	21	NOT USED.
S4	22	VERIFIES THE ERROR CORRECTING LOGIC BY WRITING DATA INTO MEMORY WITH ENABLE AND DISABLE ERROR CORRECTING, READING DATA FROM MEMORY WITH ENABLE ERROR CORRECTING AND CHECKING PROPER READ DATA AND CHECK PARITY BITS.
	23	RELOCATES THE PROGRAM FROM %10000 INTO %110000 IN MEMORY TO TEST THE REST OF MEMORY IN BANK 0.
	24	EXECUTES THE SAME TEST AS STEP 22 FOR THE REST OF MEMORY IN BANK 0.
	25	RELOCATES THE PROGRAM FROM %110000 BACK TO %10000 IN MEMORY TO CONTINUE THE DIAGNOSTIC PROGRAM.
	26	NOT USED.
	27	NOT USED.
	30 thru 47	NOT USED.
S5	50	TEST "MARCHING" HAS TWO PARTS. THE FIRST PART WRITES '1' AT COL=0, ROW=0 WITH 'ZERO' BACKGROUND AND READS BACK THEN WRITES NEXT '1' AT COL=0, ROW=1 AND READS BACK ... UP TO COL=63, ROW=63. THE SECOND PART WRITES '0' AT COL=63, ROW=63 END READS BACK ... UP TO COL=0, ROW=0. EACH EXECUTION MEANS TO ALL 16 BITS (4K RAM) AT THE SAME TIME.

SECTION NAME	STEP NUMBER	FUNCTION
S5 (cont)	51	TEST "READ-HAMMER-WRITE" HAS TWO PARTS. THE FIRST PART WRITES '1' AT THE FIRST BIT POSITION OF THE FIRST CHIP WITH 'ZERO' BACKGROUND AND READS THIS BIT AND THE 8 ADJACENT BITS 100 TIMES TO CATCH AN ERROR TO LOGGING ARRAY. THEN THE SAME IS EXECUTED TO EACH BIT OF 4K RAM OF ALL CHIPS. THE SECOND PART IS THE SAME FOR '0' WITH 'ONES' BACKGROUND.
	52	TEST "DIAGANOL" HAS TWO PARTS. THE FIRST ONE WRITES 'ONES' AT THE NW-SE DIAGONAL OF 64X64 BIT 4K RAM CHIP TOPOLOGY WITH 'ZERO' BACKGROUND. THEN READS ALL BITS TO CATCH AN ERROR IN LOGGING ARRAY. THEN MOVE THE DIAGONAL IN NE DIRECTION SO, THAT THE LEFT OVER BIT(S) STARTS IN THE SW CORNER TO KEEP THE SAME NUMBER OF BITS. THE SECOND PART IS THE SAME FOR '0' WITH 'ONES' BACKGROUND.
	53	NOT USED.
	54	TEST "PING-PONG" HAS TWO PARTS. THE FIRST PART WRITES 'ONES' AT THE FIRST COLUMN/FIRST ROW WITH 'ZERO' BACKGROUND AND READS ALL EXISTING NEIGHBOR BITS IN ROW, COLUMN AND BOTH DIAGONALS UP TO 5 IN EACH DIRECTION. READING IS IN 'TWO-BEAT' (PING-PONG) RULE. THE FIRST BEAT IS READING FROM THE CURRENT BIT AND THE SECOND BEAT FROM THE NEXT NEIGHBOR. THEN THE TEST EXECUTES THE SAME FOR THE NEXT COLUMN IN ROW UP TO THE END AND THEN FOR ALL ROWS. THE SECOND PART DOES THE SAME FOR 'ZERO' WITH 'ONE' BACKGROUND.
	55	RELOCATES THE PROGRAM FROM %10000 INTO %110000 IN MEMORY TO TEST THE REST OF MEMORY IN BANK 0.
	56	NOT USED.
	57	NOT USED.
	60	EXECUTES THE SAME TEST AS STEP 50 FOR THE REST OF MEMORY IN BANK 0.
	61	EXECUTES THE SAME TEST AS STEP 51 FOR THE REST OF MEMORY IN BANK 0.

SECTION NAME	STEP NUMBER	FUNCTION
S5 (cont)	62	EXECUTES THE SAME TEST AS STEP 52 FOR THE REST OF MEMORY IN BANK 0.
	63	NOT USED.
	64	EXECUTES THE SAME TEST AS STEP 54 FOR THE REST OF MEMORY IN BANK 0.
	65	RELOCATES THE PROGRAM FROM %110000 INTO %10000 IN MEMORY TO CONTINUE THE DIAGNOSTIC PROGRAM.
S6	66	READS CONTENTS OF BOTH ERROR LOGGING ARRAYS: LOWER 128K (LLA) AND UPPER 128K (ULA) AND REPORTS THE HISTORY OF THEM.